UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,357	02/25/2004	Brian David Johansson	A0312.70521US00	4567

7590 10/19/2005

Jamie H. Rose
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,357	JOHANSSON ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I in the reply filed on 8/22/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada (USP 5,457,420).

Note that Figure 5 of Asada shows a voltage level translator, which includes: an input signal (Vin), an output signal (Vout), external voltage (Vdd1), internal voltage (Vdd2); first and second input signal transistors (NMOS 3, NMOS 7); first and second output signal transistors (PMOS 1, PMOS 5); and a signal stabilization circuit (4, 8) comprising first (PMOS 4) and second (PMOS 8) signal stabilization transistors. Note that, for broadest reasonable interpretation, the input signal transistors (3, 4) and the first and second signal stabilization transistors (4, 8) are operated with low voltage Vdd2 so they are low voltage transistors, while the first and second output transistors (1, 5) are operated with high voltage Vdd1 so they are high voltage transistors.

4. Claims 12- 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Konishi (USP 6,373,285).

Note that Figure 1 of Konishi shows a voltage level translator, which includes: an input signal (10), an output signal (27), external voltage (voltage of supply 80), internal voltage (voltage of supply 70); first and second input signal transistors (NMOS 18, NMOS 19); first and second output signal transistors (PMOS 16, PMOS 17); and an enable circuit (14, 15) having a first state (PMOS transistors 14 and 15 are ON) and a second state (PMOS transistors 14 and 15 are OFF) in response to a signal (39) indicates the readiness of an internal voltage supply (70), wherein the signal (39) is generated from a ready-signal generation circuit (3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable Wang et al. (USP 6,650,168) in view of Asada(USP 5,457,420).

With respect to claim 10, Figure 5 of Wang et al. shows a level shifter, which includes: an input signal (in), an output signal (out), external voltage (Vddq), internal voltage (Vdd); first and second input signal transistors (N3, N4); first and second output signal transistors (P3,P4); and first and second high voltage transistors (ZN1, ZN2) that each has a zero threshold voltage. The level shifter of Wang et al. does discloses a signal stabilization circuit connected to the drains of the first and second input signal transistors. However, the Asada reference discloses a

level shifter in Figure 5 that includes a stabilization circuit (4, 8) connected to the drains of the input signals transistors (3, 4) for the purpose of improving the reliability of the shifter while maintaining the high speed of the shifter (lines 27-31 of Col. 4, and line 60 of Col. 9 to line 4 of Col. 10, Asada et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the level shifter in Figure 5 of the Wang et al. reference by providing the stabilization circuit coupled to the drains of the input signals transistors as taught by the Asada reference for the purpose of improving the reliability while maintaining the high speed of the shifter.

With respect to claims 11, Figure 5 of Wang et al. in the above modification shows a cascode circuit (N6, N7).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Konishi in view of Wang et al. (USP 6,650,168).

With respect to claim 15, the level shifter in Figure 1 of Konishi meets all the limitations of this claim (as discussed in claim 12 above) except for the first and second high voltage transistors that each has a zero threshold voltage coupled between the respective first and second input signal transistors and the respective first and second output signal transistors. However, the Wang et al. reference discloses a level shifter in Figure 4 that includes the first and second high voltage threshold transistors (ZN1, ZN2) that each has a zero threshold voltage coupled between the respective first and second input signal transistors (N3, N4) and the respective first and second output signal transistors (P3, P4) for the purpose of protecting the low voltage input NMOS transistors (N3, N4) from high voltage stress and increasing the speed of the level shifter (see line 53 of Col. 5 to line 28 of Col. 8, Wang et al.). Therefore, it would have been obvious to

one having skill in the art at the time the invention was made to modify the level shifter in Figure 1 of the Konishi reference by providing first and second high voltage transistors that each has zero threshold voltage that mediate the connection between the first and second input signal transistors and the first and second output signal transistors as taught by the Wang et al. reference for the purpose of protecting the input signal transistors from high voltage stress and increasing the speed of the level shifter.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Konishi in view of Asada(USP 5,457,420).

With respect to claim 16, the level shifter in Figure 1 of Konishi meets all the limitations of this claim (as discussed in claim 12 above) except for a signal stabilization circuit connected to the drains of the first and second input signal transistors. However, the Asada reference discloses a level shifter in Figure 5 that includes a stabilization circuit (4, 8) connected to the drains of the input signals transistors (3, 4) for the purpose of improving the reliability of the shifter while maintaining the high speed of the shifter (lines 27-31 of Col. 4, and line 60 of Col. 9 to line 4 of Col. 10, Asada et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the level shifter in Figure 1 of the Konishi reference by providing the stabilization circuit coupled to the drains of the input signals transistors as taught by the Asada reference for the purpose of improving the reliability while maintaining the high speed of the shifter.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER